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What is claimed is:

1. A memory access system comprising:

a register file having a plurality of registers each having the same predetermined bit capacity and capable of holding one or more objects depending on the bit length of the object, said registers including at least a first address register holding at least two packed objects for use in identifying respective memory addresses;

a register accessing circuit operative responsive to a memory access instruction to access said first address register in said register file;

address generating circuitry for generating at least first and second memory addresses from said at least two packed objects; and

memory access circuitry for accessing a memory using said first and second addresses.

2. A memory access system according to claim 1, wherein the first address register is an index register and wherein said at least two packed objects are offset objects for combining with a base value held in a second register in the register file to generate said first and second addresses.

3. A memory access system according to claim 2, wherein the base value comprises two packed objects representing two base addresses which are combined respectively with the packed offset objects in the index register to generate said first and second addresses.

4. A memory access system according to claim 1, wherein in the first address register, said at least two packed objects represent respective base addresses, which identify respective memory addresses when combined with an offset in a second register in the register file.

5. A memory access system according to claim 2, wherein the address generating circuitry comprises first and second addition circuits for respectively adding the

packed objects in the first register with the contents of the second register to generate said first and second addresses.

6. A memory access system according to claim 1, wherein the first register holds four offset objects, two of which are selected by the address generating circuitry for generating said first and second addresses.

7. A memory access system according to claim 1, wherein the first register holds four offset objects for use in respectively identifying four memory addresses.

8. A memory access system according to claim 1, wherein the first register holds eight offset objects, a number of which are selected for use in respectively generating a corresponding number of memory addresses for use in addressing said memory.

9. A computer system comprising:

a memory holding data objects;

a memory access unit for accessing said memory to retrieve data objects;

a decode unit for decoding instructions for use in controlling said memory access unit; and

a register file having a plurality of registers each having the same predetermined bit capacity and capable of holding one or more objects depending on the bit length of the objects;

said registers including at least a first address register holding at least two packed objects for use in identifying respective memory addresses;

wherein the memory access unit is responsive to a memory access instruction defining said first address register to access said first address register in said register file and to generate at least first and second memory addresses from said at least two packed objects, said addresses being used to access said memory.

10. A computer system according to claim 9, wherein the bit length of the data objects accessed by the first and second addresses is defined in the memory access instruction.

11. A computer system according to claim 9, which comprises a further memory access unit operable to simultaneously access said memory with the first memory access unit.

12. A computer system according to claim 11, wherein the first and further memory access units cooperate so that, when two addresses are generated by one of the memory access units, one of said addresses is issued to the other memory access unit to allow two simultaneous memory accesses to be made by the first and further memory access units.

13. A computer system according to claim 9, which includes at least one execution unit for executing data processing instructions.

14. A computer system according to claim 9, wherein the first address register is an index register, said at least two packed objects being offset objects, and wherein the register file includes a second register holding a base value which, when combined with said respective offset objects, generate said first and second addresses.

15. A computer system according to claim 14, wherein said second register holds two packed objects representing respective base addresses which, when combined with the respective packed offset objects in the first address file generates said first and second memory addresses.

16. A method of generating addresses for accessing a data memory, the method comprising:

retrieving from a base register a base value representing at least one base address;

retrieving from an index register at least one index value;

wherein at least one of the base value and the index value comprises at least two packed objects;

combining the base value and the index value to generate at least first and

second addresses for accessing said memory;

wherein said base register and index register are defined in a single computer instruction.

17. A method of accessing a memory holding data values, the method comprising:

reading a memory access instruction which identifies at least a first address register holding at least two packed objects for use in identifying respective memory addresses;

simultaneously generating at least first and second memory access addresses from said at least two packed objects; and

using said first and second memory access addresses to access said memory.

18. A method according to claim 17, wherein the first memory address is supplied to a first memory access unit and the second memory address is supplied to a second memory access unit, the first and second memory access units simultaneously accessing the memory using the first and second addresses.

19. A computer program product comprising program code means capable of cooperating with a computer when loaded therein to effect memory accesses, said program code means including a memory access instruction which identifies at least a first address register holding at least two packed objects for use in identifying respective memory addresses such that said first and second memory addresses are simultaneously generated by a computer on which the computer program product runs.